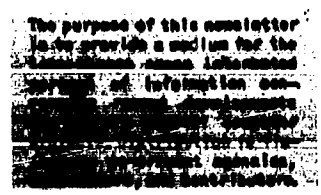
DIGITAL COMPUTER NEWSLETTER



OFFICE OF NAVAL RESEARCH · MATHEMATICAL SCIENCES DIVISION

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EDITORIAL NOTICES

EDITORIAL POLICY

The Digital Computer Newsletter, although a Department of the Navy publication, is not restricted to the publication of Navy-originated material. The Office of Naval Research welcomes contributions to the Newsletter from any source. The Newsletter is subjected to certain limitations in size which prevent publishing all the material received. However, items which are not printed are kept on file and are made available to interested personnel within the Government.

DCN is published quarterly (January, April, July, and October). Material for specific issues must be received by the editor at least one month in advance.

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The Office of Naval Research welcomes contributions to the Newsletter from any source. Your contributions will provide assistance in improving the contents of the publication, thereby making it an even better medium for the exchange of information between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to the editor for future issues. Material for specific issues must be received by the editor at least one month in advance. It is often impossible for the editor, because of limited time and personnel, to acknowledge individually all material received.

CIRCULATION POLICY

The Newsletter is distributed, without charge, to interested military and government agencies, to contractors for the Federal Government, and to contributors of material for publication.

For many years, in addition to the ONR initial distribution, the Newsletter was reprinted by the Association for Computing Machinery as a supplement to their Journal and, more recently, as a supplement to their Communications. The Association decided that their Communications could better serve its mer ers by concentrating on ACM editorial material. Accordingly, effective with the combined January-April 1961 issue, the Newsletter became available only by direct distribution from the Office of Naval Research.

Requests to receive the Newsletter regularly should be submitted to the editor. Contractors of the Federal Government should reference applicable contracts in their requests.

All communications pertaining to the Newsletter should be addressed to:

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COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

FX-1—LINCOLN LABORATORY, MASSACHUSETTS INSTITUTE OF TECHNOLOGY, LEXINGTON 73, MASS.

The fastest digital computer ever built is now in operation at the M.I.T. Lincoln Laboratory in Lexington, Massachusetts. Known as the "FX-1", this new computer is in every important respect a working model for a new generation of machines, ten times faster than any computers in general use today. The significance of the new machine lies not in its size or capacity, which are modest, but in the unusually high speed at which it operates, and in new construction techniques designed especially for high frequency operation.

It is the first machine with a main memory using thin magnetic films in place of ferrite cores for high-speed, random-access storage. FX-1 is designed to be a complete, small-scale, general-purpose computer, for realistic tests of fast logic circuitry and magnetic film storage in system operation.

In specifying the speed of a computer, there are two items of particular interest: (1) the time required to read a computer word out of the memory and to write in a new word (the "read-write cycle time"), and (2) the speed of the logic circuits, which may be specified by the rate of the timing pulses which govern the operation of these circuits (the "clock rate"). Both of these items are noteworthy in the FX-1, since in both instances the new machine is substantially faster than the most advanced commercial computers of today.

Memory

The read-write cycle time for the central memory of the Lincoln FX-1 is 0.3 microsecond. The fastest main memories in machines today have cycle times that generally range from 2 to 12 microseconds. These memories use magnetic cores for storage, following techniques developed by Lincoln Laboratory some years ago, without which the large, high-speed, general-purpose computers of today could not have been developed. The largest core memory in existence, with a capacity of more than 2,500,000 bits, was built by Lincoln some four years ago and is part of the older Lincoln TX-2 computer. This large core memory has a read-write cycle time of 8.5 microseconds.

Also a part of TX-2 is a small fast memory using thin magnetic films, the first such memory to be installed in a computer. In regular use for almost two years, this magnetic film memory operates in TX-2 with a cycle time of 0.8 microsecond, consistent with its functions in the computer itself; in bench tests, a cycle time of 0.4 microsecond was attained, limited by the performance of the transistors that were available at the time the memory was built.

The faster magnetic film main memory in the new FX-1 profits from improved transistors, circuitry and fabrication techniques that have been developed in the intervening two-year period. Various arrays of magnetic film memory elements deposited on thin glass plates are possible. Circular spots were used in the small TX-2 memory and small rectangular spots are used in FX-1.

The initial FX-1 memory has a capacity of 256 words of thirteen bits each, but provision has been made to increase the initial capacity by a factor of four. This memory is large enough to serve the purpose of FX-1, to provide a realistic test of fabrication and operating techniques on a practical scale, and at the same time to provide sufficient storage to enable the machine itself to be useful for some practical purposes. Because of the high speed of the logic circuits and the short cycle time of the memory, the FX-1 can match the performance of considerably larger conventional machines.

The memory employs printed-circuit wiring on a flexible sheet of resin-impregnated glass-fiber cloth. The arrays of memory elements, deposited on thin glass backing plates, are positioned on the wiring so that each magnetic-film element rests on the intersection of two perpendicular leads on the wiring sheet. When all the memory element arrays are in place on the lower half of the wiring sheet, the upper half is folded over to make the completed memory. This single unit contains the 256-word, 3328-bit memory of the FX-1 computer.

Circuits

The logic circuits in Lincoln's new FX-1 operate at an effective clock rate of 50 million pulses per second, ten times faster than TX-2 and other large machines currently in operation, and four times the rate of the fastest commercial machine disclosed to date. This increase in speed is made possible by high-speed switching transistors developed under subcontract, with the collaboration of Lincoln's Computer Components Group, and now in commercial production. The fastest commercial machines now in common use have clock rates comparable to that of the TX-2.

Approximately 3000 transistors are used in the FX-1; this is about the same number as in the Lincoln TX-0 computer, built about five years ago, which was the same forerunner of the TX-2 computer in use at the Laboratory today. TX-2 has some 30,000 transistors in the central machine, and one of the large new commercial machines will have as many as 200,000.

The FX-1 logic circuits are packaged in plug-in units that have been designed for compactness, as well as being particularly suited to high frequency operation. Components are mounted on or between two printed-circuit boards that are an integral part of the mechanical framework of the plug-in unit. The plug-in units are mounted in trays that hold up to 20 units each and themselves plug into the computer frame. Plug-in units with closely related functions are located on a common tray to simplify interconnections.

Approximately 325 plug-in units of 12 standardized basic types are used in the FX-1. They are mounted in 24 trays, of 13 different types. The entire computer, with power supplies, occupies only three relay racks.

Some of the trays in the FX-1 are fabricated by a developmental technique called "plated-circuit" wiring, as contrasted with "printed-circuit" wiring for the plug-in units and conventional point-to-point soldered wiring for most of the trays. The plated-circuit trays employ two layers of etched wiring sandwiched on either side of a central, copper groundplane. Wiring of this type behaves like strip transmission line, with uniform impedance characteristics that should simplify and improve circuit performance at high frequencies. Interconnections from one layer of wiring to another are made by plated-through holes rather than by soldering. The FX-1 is a good vehicle in which to test this type of wiring, where it is an important factor in the performance of high-frequency circuits.

The FX-1 computer was designed and built by the Digital Computers Group in the Information Processing Division of the M.I.T. Lincoln Laboratory, with assistance from Lincoln's Computer Components Group. Lincoln Laboratory is a center for research, operated under Air Force contract by M.I.T., with the joint support of the U.S. Army, Navy, and Air Force.

COMPUTER DEVELOPMENT—
LINCOLN LABORATORY,
MASSACHUSETTS INSTITUTE
OF TECHNOLOGY,
LEXINGTON 73, MASS.

Computer development at the M.I.T. Lincoln Laboratory had its origin in the M.I.T. Digital Computer Laboratory that grew up around Whirlwind I, the first modern, high-speed, general-purpose digital computer. Planning for Whirlwind began in 1946, and the machine was put into full-scale operation late in 1951 as the largest and fastest digital computer in existence at that time. The design and construction was sponsored by the Office of Naval Research.

Lincoln Laboratory was founded in 1951, at the request of the Army, Navy, and Air Force, to effect urgently needed improvements in air defense. The rapid evolution of computer technology during the period 1946-1951, stimulated to a considerable degree by the development of Whirlwind, made it possible to demonstrate the feasibility of a semi-automatic system to process radar data, generate displays, and guide defensive weapons. The realization of such a system for continental air defense was the major preoccupation of Lincoln Laboratory during its first 8 years of existence. The result is the SAGE (Semi-Automatic Ground Environment) System, the largest data-processing system ever attempted, now in operational use by the Air Force. This system employs some 70 large digital computers (designated AN/FSQ-7) and a much larger number of specialized data processors. All this equipment was originally designed at Lincoln Laboratory, with further engineering development and production carried out by various manufacturing contractors.

Soon after Lincoln Laboratory was founded, the M.I.T. Digital Computer Laboratory became the Digital Computer Division of Lincoln, and Lincoln assumed primary responsibility for the use and further development of Whirlwind I. In 1953-54, Whirlwind was a primary test vehicle for the first 1024-word ferrite core memory, developed to supplant the electrostatic storage tubes previously employed for high-speed storage. The ferrite core memory is an M.I.T. contribution that has proved to be of fundamental importance to modern digital computer technology. The first core memory in Whirlwind had a capacity of 1024 16-bit words, with a read-write cycle time of 10 microseconds.

Also, in 1953, the Memory Test Computer (MTC) was placed in operation, both as a memory test vehicle and as a general-purpose computer in its own right. In 1954, a 4096-word core memory was installed in MTC, with a read-write cycle time of about 5 microseconds, twice as fast as the central core memory in Whirlwind.

The Lincoln TX-0 computer was put into operation in 1956. This was the first Lincoln computer in which transistors (about 3000) completely supplanted vacuum tubes in the logic circuits. It has a 5-megapulse clock rate, two and a half times faster than that of Whirlwind or MTC. TX-0 served as a test bed for evaluation and development of transistor circuitry and of the largest core memory ever built, with a capacity of about 2.5 million bits and a cycle time of 6.5 microseconds. This memory was developed and built by Lincoln as a prototype for large memory units produced by IBM for the SAGE System. At the time there were no transistors that could supply the currents necessary to drive this core memory; hence this memory is vacuum-tube driven and uses about 1000 tubes.

Direct successor to TX-0 is the larger TX-2 computer. Completed in 1958 and still in active use, the TX-2 has about 30,000 transistors in the central machine. Both TX-0 and

TX-2 use the same general circuit design and operate at the same clock rate (5 megapulses per second).

The large core memory is now the main memory of TX-2, but two smaller auxiliary memories are also worthy of note. In 1959, a transistor-driven core memory (TDCM) was put into operation, with a capacity of 150,000 bits (4096 36-bit words) and a cycle time of 4.5 microseconds. In that same year, a small memory using thin magnetic films was installed in TX-2, the first such memory to be used in an operating computer. Very small but very fast, this magnetic film memory has a capacity of only 320 bits; however, it operates with a cycle time of 0.8 microsecond in TX-2, and has been bench tested to 0.4 microsecond.

It was at the beginning of 1959 that the SAGE-oriented parts of Lincoln's computer work were transferred to the newly-formed MITRE Corporation. The advanced computer development groups remaining at Lincoln were incorporated into the newly established Information Processing Division, with which they are presently affiliated. It is these groups that have been concerned with the development of the new FX-1 computer.

Throughout the years of its computer development, Lincoln has consistently supported and stimulated the development of higher frequency transistors, through subcontracts with transistor manufacturers. Several generations of transistors developed under this program are now commonly available and in general use. It was the 2N240 and 2N293 transistors that made possible the TX-0 and TX-2 computers, and it is the 2N769 (that has now been used at Lincoln for almost two years) that has made possible the development of the new FX-1.

No mention is made here of the many other digital computers and information processing systems that have been built for special purposes by various groups in the Laboratory. The discussion has been restricted to a selected few, general-purpose machines in order to illustrate the chronological increase in speed and capability of memories and logic circuitry. Tables I to III summarize this evolution in greater detail from different aspects.

Table I. Random-Access Memories in Lincoln Laboratory Computers

Year	Machine	Type	Bits	Read-Write Cycle Time (microseconds)
1953	Whirlwind I	ferrite core	16,000	10
1954	MTC	ferrite core	65,000	5
1956	TX-0	ferrite core	1,250,000	6.5
1958	TX-2	ferrite core	2,500,000	6.5
1959	TX-2 (TDCM)	ferrite core	150,000	4.5
1959	TX-2	magnetic film	320	0.8
1961	FX-1	magnetic film	3,300	0.3

Table II. Effective Clock Rates of Lincoln Laboratory Computers

Year	Machine	Number of Cathodes or Transistors in Central Machine	Effective Clock Rate (megapulses/sec)
1950	Whirlwind I	5,000 C	2
1953	MTC	5,000 C	2
1956	TX-0	3,000 T	5
1958	TX-2	30,000 T	5
1961	FX-1	3,000 T	50

Table III. Representative Operating Characteristics of Three Lincoln Laboratory Computers

Characteristic	Whirlwind I (1949-53)	TX-2 (1958)	FX-1 (1961)
Basic word length (bits)	16	36	12
Effective clock rate (mega-pulses per second)	2	5	50
Speed (average operations per second)	30,000	120,000	2,000,000
Memory			
Core (bits)	16,000	2,500,000	0
Read-write cycle time (microseconds)	10	6.5	-
Magnetic film (bits)	0	320	3,300
Read-write cycle time (microseconds)	-	0.8	0.3
Components			
Cathodes	5,000	1,000	0
Transistors	0	30,000	3,000
Power (kilowatts)	150	20	5

AN/UYK-1—A NEW STANDARD NAVY COMPUTER—THOMPSON RAMO WOOLDRIDGE, CANOGA PARK, CALIF.

A fully militarized, medium-scale, core memory digital computer, the AN/UYK-1 is now in operation at several Navy field installations and is available off-the-shelf from the manufacturer.

The AN/UYK-1 was developed under the sponsorship of the Bureau of Ships. The objective of the program, carried out by Thompson Ramo Wooldridge Inc., RW Division, was to develop an inexpensive, economical-to-use, digital computer for general shipboard use. The system was required to be compatible in word length and input-output characteristics with the NTDS system and with NTDS peripheral devices.

The first AN/UYK-1 was delivered and accepted by BuShips in the fall of 1961. The computer has been selected for the TRANSIT high accuracy navigational system, and has also been ordered for other military applications by both the Navy and Air Force. The new computer is particularly well qualified for real time data processing applications in remote locations or in adverse environments where exceptional reliability is required over long periods.

The AN/UYK-1 has a basic 8192 15-bit word random access core memory expandable to 32,768 words. There are over 8000 useful instructions with which to set up any desired problem-oriented macro instruction language. The AN/UYK-1 conveniently operates in multiple word lengths, and can perform floating point operations.

"Stored logic," an advanced concept in computer logical design, was used in the AN/UYK-1 to achieve a degree of versatility and operator convenience not ordinarily found in such an inexpensive computer. Stored logic permits the user to select a word length, order structure, and instruction repertoire especially suited to the problem at hand. These normally "wired in" characteristics are specified by data stored in the computer's memory and may be changed during the normal loading procedures without hardware modification. Stored logic also permits a computer to be designed with a minimum of components, thereby greatly increasing reliability and reducing cost.

What "stored logic" means to users is that they have at their command a computer intentionally designed for efficient operation in the interpretive mode. (By contrast, conventional computers are primarily designed for a particular class of problems, and can be adapted—via interpretive routines—to new classes of problems only at the cost of severe penalties in efficiency caused by the "overhead" machine operations associated with conventional interpretive routines.) To prepare an operational program for the AN/UYK-1, the programmer writes "calling sequences" as though he were

writing symbolic instructions for another machine. There are no efficiency penalties for this convenience, because instructions are always executed at machine speeds.

The following are representative AN/UYK-1 execution times:

Function	Double Precision (30 bits)	Single Precision (15 bits)
Square root	1.7 milliseconds	0.63 milliseconds
Sine or cosine	3.8 milliseconds	0.90 milliseconds
Arctangent	2.5 milliseconds	0.94 milliseconds
Arcsine	5.9 milliseconds	1.85 milliseconds

The AN/UYK-1 communicates with standard peripheral devices in 15-bit parallel words over one I/O channel and with NTDS devices in 30-bit parallel words over two other I/O channels. The computer can receive information from one device while transmitting information to another device. A system of 11 interrupt lines provides capability for the time sharing of peripheral devices to connect to and communicate efficiently with the AN/UYK-1.

The AN/UYK-1 is 59 inches high, about 20 inches wide, and 16 inches deep. It is housed in a rugged protective aluminum casting that absorbs shock and vibration and resists corrosion. The AN/UYK-1 is completely designed to military specifications. All circuits are solid state, and preferred military components are used. An extensive system of standard peripheral devices and a growing library of user programs are available to the Navy user.

UDOFTT MODIFICATIONS—U.S. NAVAL TRAINING DEVICE CENTER, PORT WASHINGTON, N.Y.

The Universal Digital Operational Flight Trainer Tool (UDOFTT) at the Naval Training Device Center, Garden City, New York is being modified to accept as input, data being supplied by a simulated submarine ship control console developed by Electric Boat Division, General Dynamics Corporation under the ONR SUBIC program. The UDOFTT computer (see DCN April 1960 and January 1958) is a high-speed, general purpose, digital computer with the added flexibility of real-time input-output channels. The system incorporated two aircraft cockpits which are activated by the computer. The prime objective of the UDOFTT program was to develop a digital computer for real-time control of operational flight trainers. Due to its flexible input-output system, UDOFTT is especially adaptable to such functions as the simulation of space vehicles, surface and subsurface vessels, and the testing of flight dynamics.

The SUBIC (Submarine Integrated Control) program for which the Electric Boat Division of General Dynamics Corporation is prime contractor was established for the purpose of achieving an integration of the information and control function within the submarine. The SUBIC program envisions a submarine control room wherein central control of the ship and its many functions would be exercised from a minimum of operator stations. The SUBIC control room will be constructed to simulate that of either an ASW or an FBM submarine. For the FBM version, there will be a maximum of seven stations designated ship control, surveillance, navigation, tactical weapons, strategic weapons, central monitoring and command stations. The ASW version will consist of a maximum of six operations stations, tentatively called the ship control, surveillance, navigation, tactical weapons, central monitors, and command stations. The FBM control room can, by making inoperative the strategic weapons station and portions of other stations, be used for ASW functions.

It is intended as the initial step in the SUBIC-UDOFTT program to install a functional research version of the SUBIC single operator ship control station for feasibility experimentation. A malfunction console will accompany this installation for use in inserting simulated casualties into the various systems controlled at the ship control console. The malfunction console will also be used for monitoring performance of the ship control console operator.

It is not feasible to simulate all seven SUBIC stations at once, because of the number of input-output channels and the size of the memory required. The UDOFTT will be programmed to simulate the complete dynamics of a submarine, and one research console at a time will be tied into the system for feasibility demonstration and experimentation.

The majority of connections between the console complex and the computer are made through the patchboard systems. The main patchboard allows computer input-output lines to be utilized either by the original flight trainer equipment or by other "external" systems, such as the SUBIC consoles. An auxiliary patchboard is used to provide access to the computer lines coming from the main patchboard for either of two "external" systems. It is thus possible, by patchboard switching and change of computer program alone, to share the computer for three functions. In addition, "external" systems attached to the output of the auxiliary patchboard can be removed and replaced by

others through screw-type connections at the output terminal box of this patchboard system.

With the patchboard systems described, access to the UDOFTT computer is obtained through:

64 Discrete Input Lines
24 Analog Input Channels of 10 lines each
64 Analog Output Lines
24 Discrete Output Lines
16 Reference Voltage Lines for Analog Outputs
4 Systems Intercommunicaton Lines
2 Systems Interlock Lines

Connection has also been made to 20 bits of a computer output register normally intended to feed a printer. The UDOFTT computer print register has been augmented with transistorized buffer circuitry to allow the use of the print register for the SUBIC simulation program. The output of the register is used to drive digital buffer circuitry which supplies information to console indicator circuits, control pulses for indicator selection circuits, timing pulses for a counter, and reset pulses. The lines from the print register buffer circuitry bypass both patchboard systems and lead directly to the circuits controlled by the signals from this register.

For communication purposes, the malfunction console has a speaker-microphone, a press-to-talk foot pedal, and a control switch. The switch can be used to turn all communications off, to permit communications between the SUBIC consoles only, between the malfunction console and the computer console only, or among the three consoles.

A similar attack is being planned for the SURIC (Surface Integrated Control) program. The SURIC program is concerned with the development of new concepts to facilitate the control by command of all functions of a surface ship. This program is being developed by Sperry Gyroscope Company under ONR sponsorship. The first console to be installed and evaluated will be the conning console which is designed to increase the performance of conning officers in vehicular control of the ship, decision making in navigation, maneuvering and collision situation, and communication with internal and external stations.

The SURIC-UDOFTT program is in the planning stage and integration plans between console and computer are not complete. Plans are underway to utilize the SUBIC Electric Boat external interface equipment.

NAVAL TACTICAL DATA SYSTEMS—
UNIVAC DIV., SPERRY RAND CORP.,
ST. PAUL, MINN.

The Univac Military Department, systems design contractor for the Naval Tactical Data System, has been awarded a letter contract for maximum liability of $19 million for the production of additional equipment. The Navy Bureau of Ships said the contract is for production of computers and peripheral equipments for NTDS shipboard installations. The contract also covers "software" services such as computer programming, installation, checkout, and continuation engineering, according to the Navy.

The Univac AN/USQ-20 computer, heart of NTDS, is the principal development in the program. This general purpose, stored program, real-time machine is severely reduced in size for shipboard use and encased in a rugged cabinet to withstand the effects of shock, vibration, and salt air.

As systems design contractor for NTDS, Univac has been responsible not only for the design, development, and production of the AN/USQ-20 and at least 20 pieces of communicating peripheral devices, but also the initial study to determine the feasibility of automated processing of tactical information in a naval combat situation.

The company also has functioned as coordinator between the Bureau of Ships and other prime contractors and government agencies. The latter include the Navy Electronics Laboratory and Fleet Anti-Air Warfare Training Center at San Diego, Calif. (where Univac maintains a permanent consignment of 145 people) and a group of naval officers assigned to NTDS.

Seventeen AN/USQ-20 computers have been delivered to the Navy. Nine are already installed and operating aboard ships of the fleet.

Military counterpart of the AN/USQ-20 is the Univac 1206 military computer, two of which have been delivered to non-Navy customers.

The 33 x 37 x 66-inch computer contains 3776 identically packaged circuit modules. Rollout drawers permit easy, rapid access to the component packages.

Its very high-speed, random access memory contains one million bits of information. Thirty bits, comprising a single word, may be extracted from any location in the memory in only 2.5 microseconds. The computer is capable of completing an instruction in 13 microseconds, or 77,000 instructions in a single second.

An expansive array of electronic data gathering devices and communicating equipments combine with the computers to form a shipboard NTDS complex. Input (tracking) information received from external sensor devices—i.e., sonar and radar—are used by the computers for target evaluation, identification of threats, determination of what types of counter weapons to employ, and assignment of weapons. The latter might include guns, missiles, or intercept aircraft.

Computers which can collect, store and evaluate tactical information, and make decisions perform these functions in a small fraction of the time required for conventional systems to accomplish the job.

An automated Navy Combat Intelligence Center (CIC) enables the units in a task force to operate as though they were one huge ship.

GE 225 AND INFORMATION RETRIEVAL—WESTERN RESERVE UNIVERSITY, CLEVELAND 6, OHIO

The Center for Documentation and Communication Research in the School of Library Science at Western Reserve University installed a GE 225 during the summer of 1961. Its main purpose is to perform literature searching and information retrieval. However, it is anticipated that time on the computer will be available for University research and student training.

With the computer, General Electric Company also delivered a program to perform the literature searching which was previously done by the Western Reserve University Searching Selector, a relay Searching Selector which was designed and constructed at Western Reserve University.

At present, some 3-1/2-million cards comprising approximately 80,000 articles in the field of metallurgy are being transcribed to magnetic tape. These include much of the journal literature from 1958 to date. More than half of this file has already been transcribed. Inquiries to these files compose retrospective searches. Current awareness searches are being conducted now on a weekly basis. The retrospective searches will begin as soon as the transcription is completed.

The 8192 word core memory with 2 tape units and punched cards in and out makes a nice configuration for much of the University research as well as student training. An assembly routine known as GAP is now being used for programming the GE 225. A compiler, which is in preparation at the General Electric Company, Phoenix, Arizona, will also be available.

COMPUTING CENTERS

NORC MEMORY PERFORMANCE—DAYSTROM, INC., ARCHBALD, PA.

In March 1960, the Navy updated its large Naval Ordnance Research Computer (NORC), which recently tracked the Soviet cosmonauts, by installing a solid-state, random access, core memory as a replacement for the computer's original CRT memory unit. A recent performance report from the Navy on the replacement memory indicates that it has more than lived up to all expectations. It has greatly improved computer reliability and reduced overall computer down-time.

The report states that for a total operating time of 12,407 hours during the period March 1960 to August 1961, mean time between failures attributed to the memory has been better than 1770 hours. During the same 18-month period, it established a down-time to total-operating-time ratio of better than 0.3 percent. During the last 6 months of operation, the ratio was better than 0.1 percent. It should be noted that much of the down-time in the early months was due to inexperience of maintenance personnel in servicing the memory. The Daystrom memory is one of the largest and fastest all solid-state memories in use today. It has a storage capability of 20,000 words, (each word 66 bits in length) and a full read-write cycle of 8 microseconds. It contains many design features including transistorized switching circuits which allow the unit to work as part of the NORC system in the same mode as the original vacuum tube and totally different type of memory which it replaced.

One of the original large high-speed digital computers, NORC occupies some 3500 square feet of floor space at the Naval Weapons Laboratory, Dahlgren, Va. It has been in almost constant operation since 1955 and can accomplish 15,000 three-address arithmetic operations per second.

In recent months, in addition to so-called "routine work," NORC definitely established

that Soviet cosmonauts Titov and Gagarin were in actual orbit around the earth. It also tracked their orbital flights and kept the world informed of their progress as they circled the globe. NORC also has handled other highly complicated assignments including guidance calculations for Polaris missiles and surveillance satellites plus dozens of other highly classified projects.

COMPUTER SIMULATION OF CITY TRAFFIC—NATIONAL BUREAU OF STANDARDS, WASHINGTON 25, D. C.

The National Bureau of Standards has programmed high-speed data processing and display equipment to simulate traffic flow over a nine-block length of a principal traffic artery in downtown Washington, D. C. After information on volume of traffic and traffic controls has been fed into the system, the simulated traffic flow is tabulated on printouts and is also shown in a motion picture of simulated cars moving, changing lanes, and stopping for lights, as in a helicopter view of the actual streets. This result has been attained in a three-year program conducted by M. C. Stark, of the NBS Data Processing Systems Laboratory for the Bureau of Public Roads.

For some time the rapid increase of traffic on city streets has been a source of concern to traffic engineers and city planners. Municipalities must assume that streets now used to near capacity will have to carry even more traffic in the future. Thus traffic experts feel that detailed studies to correct congestion points, which even now are urgently needed, may become absolutely essential within perhaps the next decade. In such studies the problem is to determine the results of proposed changes in traffic control measures without actually disrupting traffic.

Automatic data processing to determine the optimum use, timing, and placement of traffic control devices appears to offer a promising approach to this problem. Simulation runs can be made with a computer to study the sensitivity of the traffic flow to proposed changes in the signal system and to explore the capacity of an existing system to handle different patterns or increased volumes of traffic. Many other traffic engineering situations, such as use of one-way streets, banning left turns, location of bus stops, and restriction of parking, also can be studied in this way.

Previous Work

In 1956, H. H. Goode, of the University of Michigan, and his colleagues reported the use of computer techniques in traffic engineering by setting up a computer model of two north-south and two east-west streets, both two-lane and two-way. All four intersections were signal-controlled and the route (straight through, right turn, or left turn) for each car was randomly assigned at each intersection. Each car was identical to all others and was represented by one binary digit or "bit;" all moved at the same speed and maintained the same spacing between cars. Traffic flow in the Goode model was presented in motion picture form for analysis.

Configuration of Model

In 1958, the Bureau of Public Roads requested the National Bureau of Standards to conduct a traffic research study by means of a simulation model using several improvements over the earlier work as suggested by Professor Goode. The most significant improvement was the use of a computer "word" to permit the use of more variables and a planned route for each car instead of tabulating it as an undistinguished computer bit.

The model selected for use was based on a heavily traveled 0.6-mile stretch of Washington, D. C.'s 13th Street, N. W., which includes ten intersections from Euclid Street to Monroe Street. Seven of the intersections had traffic signals and three were controlled by stop signs at the east-west streets. The model includes several two-way cross streets (two at a 60-degree angle), one T-intersection, and several one-way cross streets. The study was restricted to the peak evening rush configuration in which all four lanes of 13th Street are used for northbound traffic.

Previously acquired traffic-survey information was used to determine the volume of cars traversing the entire course on 13th Street and those entering, crossing, and leaving it at each intermediate point. This permitted the computer program to show traffic composed of purposefully operated vehicles, each having a route assigned at the time of its generation.

The streets of the model were divided up into 12-foot long rectangles called "unit blocks." The unit blocks in each lane were numbered in sequence, from entrance to exit of the course and cross-wise at each side street, so that any position could be given by unit block number. The computer required the position of each vehicle for each computation and assigned a new position (if changed) as part of each computation.

Operation of Model

Vehicles of the model were "generated" at each of the possible entrances to the course by means of random number generators in proportion to their numbers in the real course. At the same time each vehicle was assigned characteristics determining its route and behavior in traffic, also by means of random number generation and in numbers corresponding to the proportions in actual traffic. Most vehicles used 13th Street as an artery, being generated below the simulated stretch and leaving it at its northern end. Each vehicle destined for the end of the course continued at its desired speed unless forced to reduce speed for traffic signals and slower traffic in the same lane; each continued in its original lane unless forced to change to avoid being slowed by overtaken vehicles.

The vehicles generated at each entrance to the model were described by two words in digital format. Characteristics determined at "launch time" included: Time of departure in 1/4-second intervals; type of vehicle—automobile, small truck, or large truck; exit point to be used in determining the route; and desired speed category—15, 20, 25, 30, or 35 mph. All of these characteristics were chosen by means of random number selection from a series proportioned according to empirical knowledge.

Additional information was added within the vehicle two-word format as the computer surveyed the entire course at 1/4-second real-time intervals. Its computations determined for each vehicle the length of its "jump", or distance traversed during an interval, and assigned to each its new actual speed and position, given by its unit block number and the hundredths of the block length to which the vehicle's nose had penetrated.

Vehicles approaching stopped vehicles in the same lane (where lane changing was not possible), a stop sign, or a red light were decelerated gradually; this took the form of 1/4-second jumps of decreasing size. A stopped vehicle was identified by its two-word digital description showing a zero jump and indicating the same position at successive intervals.

When the distance between any two vehicles in the same lane became less than the allowable net clear sight distance determined by the speed of both vehicles, the net clear sight distances for the overtaking vehicle in the two neighboring lanes were determined as part of the computations of each 1/4-second interval. The three alternatives (stay in lane, switch to right, or switch to left) were evaluated at each interval, and the one chosen was the one which best permitted the desired speed to be attained. The overtaking car was switched to the lane selected by being moved through progressive intermediate straddle positions during the time required to make the change. Vehicles obliged to stay in the same lane were gradually decelerated to the speed of the leading vehicle.

The routes assigned to vehicles at the time of generation determined their behavior in complex intersection situations. Westbound vehicles were not permitted to turn left (13th Street being one-way northbound) and hence could always proceed through or make a right turn in the lane determined by route or lane preference assigned at time of generation. Eastbound vehicles assigned a turn onto 13th Street were obliged to await a gap in westbound traffic. Those requiring a near or far lane because of a later turn waited to enter 13th Street on the appropriate lane. Those not assigned a later turn entered on the preferred lane (1 or 4), except for vehicles having a LANE 4 preference, which if blocked by oncoming traffic went on to enter at LANE 1, waiting there to turn if necessary.

Vehicles assigned a turn off of 13th Street were "coaxed" into the appropriate lanes when within 1200 feet (100 unit blocks) of the turn. A definite pattern of "last chance" unit blocks for each lane shift approaching each intersection was programmed into the computer. The cars made the necessary shifts in as rapid succession as possible when approaching the turning point, following the lane-switching rules.

Computer Operation

The computer operation was performed by first programming the "rules of the road" into a high-speed computer and "filling" the model course with vehicles in a preproduction run. Several computer runs, each of three complete 80-second traffic light cycles (four minutes), were made. Sixty minutes of computer time was needed to process each run because of the many computations required—as many as 500 (in the complex lane-changing situation)—for more than a hundred vehicles each 1/4 second.

A magnetic-tape recording of the simulation and four tabular printouts were obtained from the computer; all were used in later analysis. One of the printouts, the VEHICLE GENERATION TABLE, gives for each vehicle the launch time, the exit, the type of vehicle (car, truck 1, truck 2, or marked vehicle), the generating point, the desired speed, and the lane preference. Another printout, the STATION B CHECK, tabulates vehicles passing the maximum-load point of the course for comparison

with empirical data. The third printout, the VEHICLE RETIREMENT TABLE, tabulates the individual running times and actual speed of vehicles completing the course in each lane, also for comparison with empirical data. Finally, the MARKED CAR CHRONOLOGICAL PRINT-OUT gives the location of each marked car every 1/4 second for analysis of its progress.

The magnetic tape obtained from the computer was used to make a motion picture film of the simulated model in operation, resembling a helicopter view of traffic flow on the course. The tape supplied the input to the Bureau's SEAC computer, which operated an oscilloscope to produce a visual presentation of the computed vehicle movements. This presentation was retained for repetition and analysis by triggering a 16-mm motion picture camera, mounted in front of the oscilloscope, for four frames to depict the situation at the completion of each 1/4-second real-time computation. The processed film, when projected at 16 frames per second, shows the simulated traffic movement in the model for the 4-minute run in real time.

Analysis of Results

Analysis of the tabular data and the film showed that the computer program caused the "vehicles" to behave in what seems to be a very realistic manner. They stopped at red lights, yielded right of way at stop signs, moved at various speeds, maneuvered for turns and to overtake slower cars, and formed queues when necessary; in short they did most of the definable things that are done by real cars in city traffic. During runs of the model, vehicles actually came to a stop if they reached the last chance position without making the lane shift, just as seen occasionally in real traffic.

The simulation technique has produced a model which apparently can be made to correspond reasonably well with actual field situations. Thorough evaluation of the model will require new field data, as traffic on 13th Street has changed considerably since the original counts were made. When validated, this technique will be useful in predicting the detailed effects on traffic flow due to changed parameters—moved or removed bus stops, altered signal light timing, and the like. Computer simulation will make possible, experimental manipulation of traffic situations without the possibility of snarling the real traffic. Most important, experimental manipulation of traffic loads in models of today's streets should make it possible to estimate how long these streets can be used without change and to predict what changes will then be needed.

AEC COMPUTING AND APPLIED MATHEMATICS CENTER—NEW YORK UNIVERSITY, NEW YORK, N. Y.

An IBM 7090 has replaced the IBM 704 at this center, and the present peripheral equipment will be replaced by an IBM 1401. The 7090 has:

32 K Storage
2 Data Channels
7 Index Registers
12 729-IV Tape Units (As many as 4 of these can be connected to the 1401)
Card Reader
Card Punch
Printer

Furthermore, the 7090 has 2 new instructions, Enter Significant Mode (ESM) and Test whether in Significance Mode (TSM). The latter also causes the machine to leave the significance mode of operation. If an ESM has been executed, the results of floating point operations will be numbers in standard floating point representation, but with just enough leading zeroes in the fractional part so that all the remaining bits are significant. If an ESM has not been executed, the 7090 will do floating point operations in its usual manner.

COMPUTER TRAFFIC CONTROL—TRW COMPUTERS CO., CANOGA PARK, CALIF.

A digital computer system will be used to help control vehicular traffic in Los Angeles this spring. From a control center in City Hall, the computer system will monitor 4 miles of Sunset Boulevard west from downtown Los Angeles and regulate traffic signals in response to vehicular flow.

The computer, a Thompson Ramo Wooldridge RW-300, is capable of analyzing and directing traffic patterns, and reacting instantaneously to changing traffic conditions on the crowded boulevard. This pilot system, which will mark the nation's first use of a digital computer by a city for traffic signal control, will be gradually expanded to control more and more of the critical intersections in congested areas of Los Angeles.

The installation of this computer system will help speed the day when traffic control in Los Angeles will be able to keep pace with the ever-increasing volume of vehicles on the city's thoroughfares. This joint effort of the City Traffic Department and the traffic control experts of Thompson Ramo Wooldridge is another

step in the overall Los Angeles redevelopment plan.

The computer will receive traffic volume and movement information, transmitted by telephone lines, from automatic detectors located within and at the borders of the controlled section of Sunset Boulevard. By using this data and an analysis program stored in its memory, the computer will continuously decide on the best settings of the traffic signals. These decisions, transmitted back to the intersections, will control the signals to provide the most effective flow of traffic.

By utilizing the experience gathered on the traffic flow from this 1 percent of the city's intersections, future traffic problems can be accurately anticipated and computer control may be readily expanded to meet these forthcoming needs.

The high speed of the RW-300 computer and the ease with which it can communicate with the signal lights at a great many remote points, allows the computer to be extremely adaptable to analyzing and alleviating some of the complex traffic problems of Los Angeles.

The downtown area of Sunset Boulevard chosen for the initial application of computer control is not only a major thoroughfare, but is also an important bypass for a heavily traveled section of the Hollywood Freeway. Furthermore, Sunset Boulevard experiences a variety of peak flow traffic patterns as a result of many downtown special events.

Sunset Boulevard is a major thoroughfare in its own right. In the central city, it lies substantially parallel to the Hollywood Freeway. With the computer control system, Sunset Boulevard can be developed as a highly effective signalized thoroughfare to relieve the Hollywood Freeway, and to serve as an emergency route when the freeway is closed for any reason.

Thus, one objective of the new signal control system on Sunset is the development of major thoroughfare capability. Another objective of the Sunset Boulevard installation is to raise it to the standards set for major thoroughfares in Los Angeles.

Two principal policies are considered by cities when they modernize their traffic control systems: (1) to provide a centralized control system; and (2) to provide a system responsive to traffic needs. Some cities have adopted one of these objectives, some the other. The City of Los Angeles, in its traffic modernization program, of which this Sunset Boulevard pilot installation is a part, has adopted both, thereby becoming the first city in the nation to take this parallel approach using a digital computer.

By locating the control center in City Hall, the City Traffic Engineer will be able to supervise traffic movement more effectively, and maintenance of the master control equipment will be made highly efficient. By making traffic signal control responsive to traffic needs, Los Angeles is attempting to utilize its street system to the greatest efficiency, thus increasing street system vehicular capacity, establishing a high level of service to motorists, reducing vehicular operating costs, and improving the safety of vehicular travel.

Basically, the system will regulate traffic flow by controlling lights relative to traffic volume. For a single light, such control would be relatively simple. Vehicle sensors in the four streets that meet in an intersection could be used to actuate a master controller that would regulate light cycles in response to the number of vehicles detected. One type is the treadle-type vehicle detectors that are often used on side streets, and sometimes on all four streets, at an intersection. These detectors are used as inputs to vary the basic fixed cycles of the lights at the intersection.

For a number of lights, however, such single intersection control has little relation to the overall traffic pattern. To control this traffic pattern most efficiently, each light must be controlled in a way that is responsive to the entire traffic flow. For this control to be efficient, a central system that senses the traffic volume at a large number of points and controls the signals in response to that mass traffic flow, must be utilized.

The TRW system to be installed on Sunset Boulevard will combine the best features of both traffic control systems described. That is, each of the controlled intersections will have its own local controller; this controller will time clearance intervals, pedestrian walk intervals, and other fixed-length intervals. The computer, in turn, will control the green intervals at each intersection, informing the local controller when to establish the cycle, split, and offset appropriate to existing conditions in the overall traffic pattern.

Twenty-six signal lights along Sunset, from Alameda to Hoover Boulevard, and 10 lights on approach streets will be controlled initially by the computer system. Two of the intersections to be controlled are three-phase intersections.

At a number of locations, detectors will count the traffic entering the controlled section

of Sunset Boulevard and at important locations within the section. Detectors to be used in the system will include pressure-type vehicle detectors and electronic detectors. These counts will be transmitted by leased telephone lines to the RW-300 digital control computer at the control center in City Hall.

The computer, making use of established control techniques and techniques that will be developed in future as a result of this and other research, will compute the appropriate signal timing for the traffic signals on Sunset Boulevard. This timing information will then be transmitted to the traffic signals.

Side street detectors will be employed at several locations to detect the arrival of traffic from side streets into and through the system.

Control circuits at each intersection will time clearance intervals, pedestrial walk intervals, and other fixed-length intervals. These controllers will also have the capability for carrying out fixed-cycle operation.

The computer will control the green intervals at each intersection, establishing the cycle, split, and offset appropriate to existing conditions. (Cycle is the time for one complete change of signals; split is the apportionment of cycle time between the streets that meet at the intersection; offset is the time difference between cycles at successive signal lights.)

The RW-300 computer is a general-purpose, magnetic-drum storage, stored-program serial machine. It is fully transistorized for maximum reliability. The computer is modified for traffic applications to provide counters for accumulating data from the system detectors, and to provide additional instructions applicable to traffic control.

The RW-300 digital control computer provides the advantages of exceptional availability in excess of 99 percent in around-the-clock service, and high-speed response—hundreds of calculations per second. Furthermore, any radical changes in traffic or topographical conditions will not obsolete the computer, but will merely require changes in the computer's program.

The computer has the ability to store a wide variety of programs to take care of special situations. The computer can decide when any of these special programs shall become effective, based on criteria established by the traffic engineer. For example, one or more special programs are expected to be developed for handling unusual weather conditions. The unusual traffic patterns that occur during athletic events can also be handled by the computer. In each of these situations, as well as in its operation with daily traffic, the computer's stored program can be prepared to handle the abnormal traffic flow in the optimum manner.

TRW will prepare the initial computer program and train city personnel in its use.

The computer system will have unused memory capacity that can accommodate traffic signals at many additional intersections at other locations within the city. This extra capacity could alternatively be used to control traffic on the nearby freeways, by controlling the access roads to the freeways.

For several years TRW has been especially interested in the development of systems for the solution of traffic problems. For some time now it has had an Automobile Traffic Control Section working full time on studies and the application of digital computers to this ever-increasing problem. The personnel within the section have blended an advanced knowledge of computer technology with many years of experience in traffic control.

The traffic control installation is the result of a 2-year study conducted jointly by the Los Angeles Department of Traffic and Thompson Ramo Wooldridge Inc. The TRW computer to be used has been extensively proved in on-line control of many chemical plants, oil refineries, cement plants, power generating stations, and missile testing facilities.

This installation is one of three computer traffic control systems engineered by Thompson Ramo Wooldridge. An RW-300 computer was previously used by the Federal Aviation Agency for over a year in the study of problems of air traffic control. A pair of TRW-330 computers will soon be installed on one of the nation's most heavily-traveled thoroughfares for control of toll registration.

"DOES ALL" INTERPRETATIVE ROUTINE—U. S. ARMY CHEMICAL CORPS BIOLOGICAL LABORATORIES, FORT DETRICK, MD.

An interpretative routine for the Univac Solid State 90 was written with two objectives in mind. First, to speed the return of computer service by shortening programming time. Second, to enable nonprogrammers in need of high-speed computations to write their own programs. To free the latter from any attention to decimal placement, all calculations are done

in floating point. The routine accepts instructions in the form of an 8-digit English mnemonic. Its repertoire of 27 instructions includes the common logarithmic, exponential, and trigonometric functions. Current use of the routine indicates the objectives have been met.

MEDLARS INFORMATION STORAGE AND RETRIEVAL SYSTEM—U.S. DEPARTMENT OF HEALTH, EDUCATION, AND WELFARE, Washington 25, D. C.

Public Health Service announced that a contract has been signed with General Electric Company for the development of an electronic information storage and retrieval system at the National Library of Medicine, to be known as MEDLARS (Medical Literature Analysis and Retrieval System).

The new computer-based system will enable the National Library of Medicine to broaden and accelerate its services to medical education, research, and practice. The Library, which this year observes its 125th anniversary, is responsible for acquiring, indexing, storing, and disseminating world literature relating to the medical sciences. The Library has the largest collection of scientific medical literature in the world.

The basic publication of the National Library of Medicine is the Index Medicus, a monthly bibliography of world medicine literature which during the past year listed some 125,000 items representing scientific publications of 77 different countries in 30 languages. The Library also publishes special bibliographies and conducts an inter-library loan service which has disseminated as many as 11,000 separate articles, on request, during a single month.

The MEDLARS system is a pioneering venture in relation to conventional library practices. There have been other efforts in the bibliographic field, with systems using electronic computers, but none approaching the size of this one. MEDLARS will be designed to process several hundred thousand pieces of bibliographic information annually.

The present system, which is part manual and part mechanized, is designed to turn out a single product—the Index Medicus. In contrast, MEDLARS will give the flexibility needed to meet other national requirements. It will be possible to produce by machine, quickly and efficiently, specialized bibliographies to meet specific requests. If someone asks for a bibliography of publications on a single disease category, for example, MEDLARS will be able to sort out and reproduce a list chosen from over a million possible articles in a very short time.

It is estimated that the development, installation, and testing of the MEDLARS project will take about 2 years. The new building of the National Library of Medicine adjacent to the National Institutes of Health in Bethesda, Maryland, which will be ready for occupancy late this year, will be adapted to incorporate the MEDLARS equipment.

DIGITAL COMPUTER DIVISION—U.S. NAVAL ORDNANCE LABORATORY, CORONA, CALIF.

The IBM 7070, which has been in operation for 8 months, was installed and accepted in January 1961. The system configuration as presently installed is as follows:

Core Memory	- 5000 words
7 Magnetic Tape Units	- 729 Type II
Card Input	- 500-cpm Reader
Card Output	- 250-cpm Punch

The computer is being used on a single shift basis in performing the Laboratory's scientific and technical data processing workload. The 7070 replaced a government-owned Burroughs 205, which, for some time, had been inadequate to handle the computational requirements of the Laboratory.

The Laboratory's computational workload arises from four principal categories of problems:

Missile Flight Data Processing

The processing of photographic and telemetered missile flight data accounts for approximately 25 percent of the computer's workload. Field and flight test data is processed on missiles during the contractor development stage and continues to be processed as the missile program progresses to final fleet usages.

Typical data processes are radar boresight camera data, photo-theodolite camera data, dial box data, sampled FM/FM and commutated telemetered data, Mitchell camera data, and drone pod camera data.

Production and Surveillance Data Processing

The processing of production data for the quality assurance program and of surveillance

data on field test information for the reliability and readiness programs accounts for another 40 percent of the Laboratory's workload. One of the larger jobs in the Information Storage and Retrieval area involves the up-to-date maintenance of complete and uniform records of all tests made on TERRIER, TARTAR, TALOS, SIDEWINDER, SPARROW, and BULLPUP missiles. Various periodic reports and special summaries are extracted from the files.

In order to provide an effective information storage and retrieval capability, the Variable Information Processing (VIP) System has been implemented on the 7070. This system combines general applicability, flexibility, unrestricted content, and speed in such a way as to provide an extremely versatile and effective information storage and retrieval system. VIP is currently being utilized for information on eight missiles which is supplied on thirteen different data collection forms.

Lethality Analysis

The detailed analysis of the effectiveness of warheads against target aircraft under various circumstances of encounter is carried out in support of the Laboratory's fuze development program. This lethality analysis work comprises approximately 10 percent of the workload being performed.

Miscellaneous Scientific Computation

The remaining miscellaneous scientific computations are composed of problems of which the following are typical:

Computation of band structure and water and carbon dioxide

Reduction of spectroscopic data

Tables of emissivity measurements

Bond strength calculations

Processing radiometric measurements of the sea

Missile data handling system simulation

Plans are being made currently to convert the 7070 from a card-oriented to a tape-oriented system by the addition of an IBM 1401 to the computer faculty.

COMPUTATION CENTER—U.S. NAVAL WEAPONS LABORATORY, DAHLGREN, VA.

The first computer program for PERT (Program Evaluation and Review Techniques) was written by the Naval Weapons Laboratory and placed in operation in 1958. While the original PERT was intended for monitoring and expediting the Fleet Ballistic Missile program, the value to management of the PERT concept has since been widely recognized and applied in Government and industry; applications by this laboratory have included Eagle-Missileer, Big Dish, and NASA projects. The original PERT program for the NORC computer has been frequently revised to increase processing efficiency and usefulness of the output. A still more flexible and efficient version for the IBM-7090 was placed in operation June 1961. Present PERT programs deal primarily with time schedules; a new program is being planned which also includes cost data.

AERODYNAMICS LABORATORY—U.S. NAVY DAVID TAYLOR MODEL BASIN, WASHINGTON 7, D. C.

The David Taylor Model Basin's Aerodynamics Laboratory has added a 2nd Alwac III E (see DCN, October 1958) for use in its wind-tunnel data reduction and research work. Absence of any definitely superior, second-generation computers in production for under $100,000 was a principal factor in this choice. Also the reliability advantage of two identical computers will more than double the Laboratory's previous computing capacity. Of interest also, is the recent running of a first production program compiled by ALSAP-1, a compiler written by E. Manderfield of Alwac and J. E. Blalock of the David Taylor Model Basin. ALSAP-1 accepts computer-oriented language and compiles a machine-language, floating-point program.

COMPUTERS AND CENTERS, OVERSEAS

ALGOL 60 COMPILER—FACIT ELECTRONICS AB, SOLNA 1, SWEDEN

An Algol compiler, the first in Sweden, has recently been completed for the FACIT EDB computer of Facit Electronics AB. The language used is Algol 60, except the symbol own and recursive procedures; there are also some restrictions on variable index bounds for arrays, expressions called by name and length of identifiers. The present compiler uses only the central unit of the FACIT EDB-core storage of 2000 words, drum storage of 800 words, and input-output of 5-channel paper tape. The programs are written direct in Algol 60 Reference Language with the limitations mentioned above and converted into the appropriate hardware representation by the punch typist. The compilation results in an effective machine code program and is quite fast. A program of 200 declarations and statements takes about 10 minutes to compile, about half of this time is used for input of the compiler and output of the object program. The compiler had been used and tested for some months before its release on February 1, 1962. An extended version using magnetic-tape and external-core storage, and with facilities for large-scale data processing, is being considered at present.

ATLAS—FERRANTI LTD., MANCHESTER AND LONDON, ENGLAND

The fact that the Atlas (see DCN, October 1960) is the most powerful computer in the world does not mean that it is a kind of colossus, set apart, to be approached only for very special purposes. The most impressive thing about this machine is the fact that the work exists for it to do; its huge capacity for calculation and data processing can already be satisfied. Atlas has been built, not to break a record, but to meet a demand.

People not familiar with the computing field may not realize the extent to which existing machines are being swamped with work. As an example, one Pegasus computer in the Ferranti Computing Service, if allowed, could be kept entirely occupied, night and day, with the work of two or three existing customers. In practice its time is rationed out to a good many more clients. Mercury machines, the fastest hitherto built in Europe, are unable to cope with some of the vast calculations required by the scientific establishments in which they are installed.

There is obviously a need for more powerful computers. Since there is no point in making a small jump when a big jump is technically possible, the Atlas has been designed to provide the greatest computing power that can be obtained at reasonable cost. Making this big technical jump forward (Atlas is 100 times faster than Mercury) is, in fact, one of the means by which the reasonable cost is achieved. This is because the value for money obtained in computing power rises roughly in proportion to the square of the actual price of the machine—an economic fact of computer manufacture.

Apart from the advantage given by this "natural law," the low price of computing on Atlas is also partly due to the great economy and ingenuity of the technical design. Many of the jobs which in other computers require expensive special circuits, for example, to control associated punched-card machines, are dealt with in Atlas by internal programmes obeyed simply by the main control unit of the computer itself. This is an economy made possible by the very high computing speed, and full advantage is taken of it in the Atlas design.

To ensure that maximum utilization of the computing power is obtained in practice, the designers have also exploited modern programming techniques to the full to organize the machine's internal flow of information in a better way. The manner in which a computer has to shift large masses of information about at high speeds in many different directions is rather like a big city in the "rush-hour." A great deal of organization is needed to make the system run smoothly and to get the commuters, or numbers, to their destinations with minimum delay. In Atlas, this organization is provided by a "supervisor programme" kept permanently in the machine.

Thus, although an Atlas installation costs something in excess of a million pounds to buy, it provides the lowest cost per computing operation that has ever been made available to the user. This is the real significance of Atlas being the most powerful computer in the world.

The improvements in organization are not simply rearrangements of existing types of electronic "building blocks." They have been made possible by radically new techniques in electronic circuitry, developed by Professor Tom Kilburn and his team at the University of Manchester. These techniques take the currently-available electronic components and

methods of construction to the very limit of their performance in speed of operation—a limit set by the rate at which electrical signals can be transmitted along wires (almost the speed of light).

Atlas can, in practice, perform about a million simple operations (additions, for example) per second. More complex operations (like multiplication) are performed at about 300,000 per second. The machine has a word length of 48 binary digits; this can be used for fixed-point numbers (40 digits long), for floating-point numbers (8 digits for the exponent), for alpha-numerical data (eight 6-bit characters), or for programme instructions (10 digits for the function part, the rest for various addresses).

A variety of input and output equipment is available, including magnetic-tape stores capable of transferring data at 90,000 characters per second. By the use of its time-sharing facility, a common feature of most modern fast machines, the computer will allow transfers of information to take place between itself and up to 20 peripheral units and 8 magnetic-tape units simultaneously.

One of the main design improvements in the Atlas is the method of achieving rapid transfers of information into and out of the high-speed store. Physically the main store consists of a high-speed magnetic-core store backed up by magnetic drums of slower access, but much larger capacity. In orthodox computers, transfers of information between the two have to be organized by instructions written by the programmer, but in Atlas the whole job is taken over by a built-in automatic system. As a result, the programmer does not have to think about two distinct stores, but simply works as if there were just one high-speed single-level store of large capacity.

This simplicity of use is achieved by what is called a "page address" system for the stored numbers and instructions. Here the numbers do not have addresses signifying particular, physical positions in the stores. They are identified simply by being in particular blocks of numbers called "pages" at particular positions in those blocks. These "pages" themselves have no fixed locations, but are moved about according to which "page" is needed in the high-speed core store for computing operations. The automatic system keeps a running record of where the "pages" are physically, so that when a programme calls for a number at a particular address it can always be found. With time-sharing operation this system allows the Atlas to switch available storage space in the most efficient way between the various programmes so as to reduce waiting time for this space.

For example, if the system transfers a block of information belonging to Programme 1 from the drum store to the core store, the space left on the drum does not have to remain empty to receive back the same block; it may well be used by the automatic system to take a different block of information belonging to Programme 2. When the Programme 1 block is no longer needed for computing it is then sent back to occupy another space which has become available.

Another feature of the main store which contributes to the high computing speed is a means by which the instructions can be "overlapped" in time to some extent. This is made possible by providing several distinct paths of access to different parts of the high-speed core store.

An important feature of the electronic design is a special "fixed store" which holds about 250 internal programmes used for various arithmetic and control operations, in fact all the operations normally found in the subroutine library of any well equipped computer. These internal programmes are called into action by special "extracode" instructions written in the main programmes.

Another important electronic design feature is the special circuitry which makes the high arithmetic speed possible. Essentially this is a new type of adding circuit with an extremely fast "carry" operation. It ensures that the "carry" process is always completed within the very short transfer time of Atlas, which is only a fraction of a millionth of a second.

In common with all modern computers, the electronic circuitry of Atlas is constructed from transistors and other semiconductor components and these are mounted on plug-in packages for ease of maintenance. Comprehensive test routines, held in the fixed store, are regularly brought into operation on a time-sharing basis during suitable intervals caused by transfer processes in the main programmes.

ALGOL—INSTITUT FUR ANGEWANDTE MATHEMATIK, JOHANNES GUTENBERG-UNIVERSITÄT MAINZ, MAINZ, GERMANY

ALCOR MAINZ 22, the final ALGOL translator for the Z 22 has been finished and in

operation since July 1961. The translator handles ALGOL with some unimportant restrictions.

ALCOR MAINZ 2002, the ALGOL translator for the Siemens computer 2002 with 2000 words magnetic-core storage and 10,000 words magnetic-drum storage has been completed and in operation since December 1961. The translator handles ALGOL 60 with minor restrictions (ALCOR, convention of 11 October 1961).

NEW COMPUTER—NORWEGIAN DEFENCE RESEARCH ESTABLISHMENT, LILLESTRÖM, NORWAY

Norwegian Defence Research Establishment, Division for Telecommunication, Lillestrom, Norway is developing a special purpose digital computer for real-time signal processing. It is intended for extraction of weak signals from noise. A set of 25 different digital and analog-digital printed circuit modules are used.

MISCELLANEOUS

FLOATING PUNCH KEYPUNCH—BUREAU OF THE CENSUS, WASHINGTON 25, D.C.

A new card punching technique has been developed by the Machine Tabulation Division of the U.S. Bureau of the Census by modifying an IBM 027 card punching machine.

This technique is called "Automatic Floating Point Punching." It provides a method of reducing the number of digits required to express a number in a punch card. The machine automatically punches the first three significant digits into the first three columns of a field and a count of the remaining digits into the fourth column.

The number keyed and the resulting punching are as follows:

Values	Punched
7	0070
24	0240
638	6380
4836	4831
12764	1272
622487	6223
4987235	4984
54332960	5435

This 027 keypunch, modified to do the floating point punching, punches left-hand zeros automatically. The verification of this type of punching is done on the same machine and is under program card control. This program is based on using an eight digit maximum number and reducing it to a four column field. This combination can be changed to meet other specifications. The fields to be punched by this method are controlled by the program card and the operator requires no additional instruction.

Because of the standard field size, a standard card form may be designed to fit the requirements of any subject matter to be punched. The punch card is now released from the fixed field format by the addition of a two digit code to identify the four column data field. This advantage is greater on data to be recorded on magnetic tape since all of the columns of a card could be filled. The information on the tape is now continuous without the blank portions normally found on the fixed field card-to-tape method. Since the data fields in the card are the same, all data related to one record is punched in sequence and columns of the last card. The computer can use this count as a check in determining if all information for a record has been received. The computer can also restore the number of digits dropped and round off the floating point number.

PLATO II—UNIVERSITY OF ILLINOIS, URBANA, ILL.

Introduction

PLATO[1] is the name of a research project in the field of multiple-student machines currently under way at the Coordinated Science Laboratory of the University of Illinois. The main aim of the project is to develop an automatic teaching system sufficiently flexible to permit experimental evaluation of a large variety of ideas on automatic instruction.

The goal of project PLATO is to be realized by constructing a series of machines, each em-

[1] PLATO: Programmed Logic for Automatic Operations.

bodying refinements indicated by experience with earlier models. PLATO II differs from PLATO I[2] primarily in its ability to instruct a number of students concurrently. The teaching logic employed in PLATO II resembles that of PLATO I in most essentials. For completeness, a resume of this logic is presented in the section titled Programmed Logic. The device is considered a multiple-student machine in the sense that one digital computer, using specialized input-output equipment, handles the instruction of several students simultaneously. The computer employed in PLATO II is ILLIAC, a medium-speed digital computer with high-speed memory of 1024 words. Because of this limited memory capacity, PLATO II can be used to instruct only two students, though the program is written to handle many more.

In PLATO II, executive control over the system as it instructs the students is exercised by a single, central computer. A teaching system such as PLATO II, in which as many functions as possible are centralized in one fast, large-scale computer, has several advantages over one which duplicates many smaller, special-purpose pieces of equipment. These advantages pertain to the power and flexibility inherent in the centralized system:

1. PLATO II makes available to every student the considerable computational resources of a large-scale, fast, digital computer. This can be of great advantage in some subject matters. For example, in certain branches of mathematics or physics, the computer can relieve the student of numerous necessary, but routine, calculations; or, it can quickly plot for the student graphs of his solutions to equations.

2. In PLATO II, the teaching logic is determined by programs within the central computer. Therefore, changes in the teaching logic can be realized by modifying or rewriting computer programs. No changing of equipment need be undertaken. This flexibility in teaching logic is particularly important in an experimental program.

3. As the machine teaches, it automatically keeps detailed records on each student's progress through the material. These large amounts of data may later be sorted and suitably processed by the same central computer. The combination of a system teaching large numbers of students concurrently and a digital computer for large-scale data processing should prove to be a powerful tool in educational research.

Description of Equipment

Figure 1 shows the general organization of equipment in PLATO II. Executive control over the system is exercised by ILLIAC, the University of Illinois' general purpose, medium-speed, digital computer. ILLIAC has a high-speed electrostatic memory of 1024 40-bit words and an auxiliary magnetic-drum storage of 10,240 words. Its speed is typified by an add time of 75 microseconds and an average multiplication time of 700 microseconds. The use of more modern computers, which are both faster

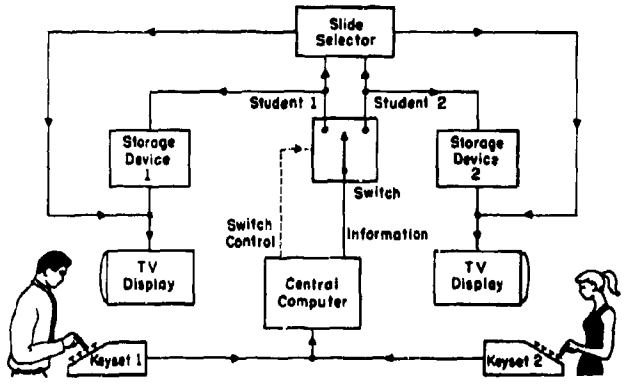

Fig. 1. General organization of PLATO II

[2] Bitzer, Braunfeld, Lichtenberger: PLATO: An Automated Teaching Device. (To be published in the IRE Professional Group on Education).

and larger by at least an order of magnitude, should make it possible to employ a greatly improved and expanded teaching logic.

Each student communicates to PLATO II by means of his own keyset. The keyset, resembling a typewriter, has keys for all alphanumeric characters; additional keys for special symbols can easily be added as needed. Thus the student can transmit numerals, words, sentences, or algebraic expressions to the machine. The student controls the machine's presentation of material by means of special keys to be described in detail later.

The machine communicates with the students by means of closed circuit television. Each student is provided with his own television screen on which the results of two separate video sources are electronically superimposed. These sources may conveniently be thought of as an "electronic book" and an "electronic blackboard." The electronic book is shared by all students, though, at any given time, different students may be using entirely different parts of it. It consists of a set of slides (containing the instructional material) which are continually scanned by a special flying-spot scanner (cf. Fig. 2). On command from ILLIAC, an electronic switch (slide selector) connects the video output from any desired slide to the appropriate student's display. The electronic book currently has a capacity of 61 slides (to be expanded to 122); the slide selector can switch from any slide in the set to any other in about 1 millisecond.

In addition to access to the book, each student is provided with his own individual electronic blackboard in the form of a storage tube. ILLIAC, by transmitting coordinates of individual points, may write characters, figures, graphs, or the like, directly onto any such tube. The tube is then scanned by the television sweep and the video thus derived is mixed with that coming from the book. Approximately 45 characters per second can be written on the student's screen by this means; 1/4 second is required to erase the entire contents of the storage tube.

In general, the electronic blackboard is used to display all material which cannot be pre-stored on slides because it is generated in the course of the lesson itself. For example, when a question is asked on a slide, the electronic blackboard makes it possible for the machine to display the student's answer superimposed on the slide in an appropriate place.

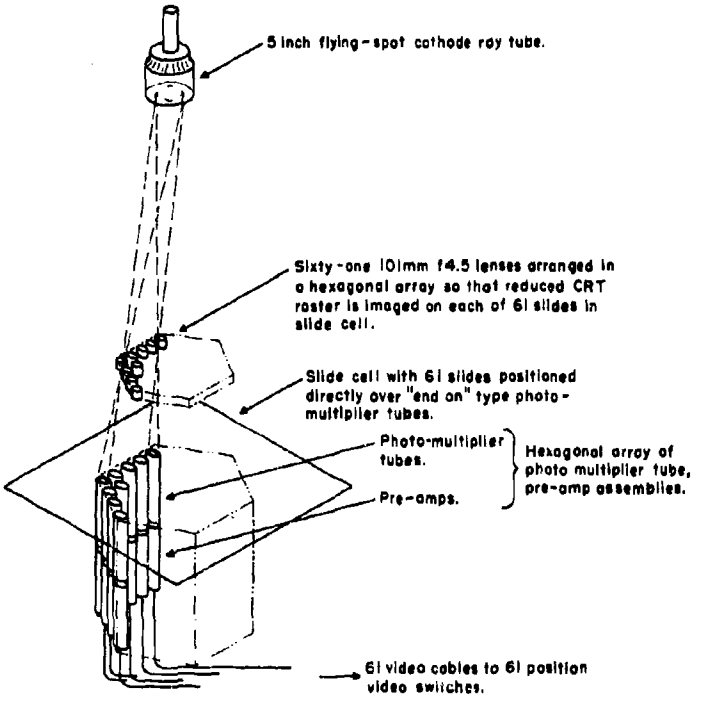

Fig. 2. The 61-slide, simultaneous scanner for PLATO II

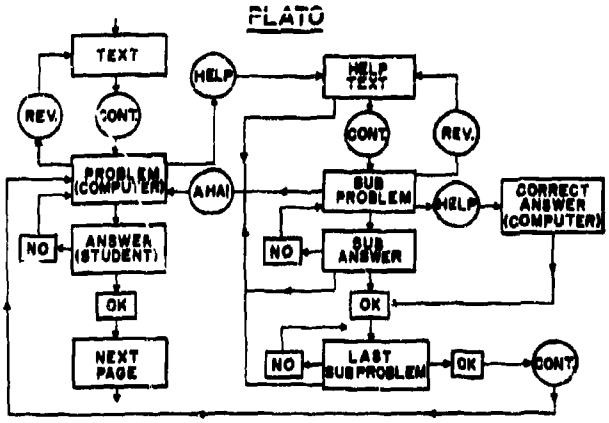

Fig. 3. Teaching logic for PLATO II

Thus, the student is able to see and study his answers in their context within the lesson.

Programmed Logic

Whereas the material to be taught is contained on a set of slides, the logical rules governing instruction are determined by programs within ILLIAC. These programs have been written to accommodate a variety of subject matters; for example, the computer program described here has been used for demonstration lessons in mathematics and French verb endings. To change courses on the machine requires only that the slides of the electronic book be changed and a suitable parameter tape be read by the computer; the basic program remains the same.

The PLATO II computer program requires each student to proceed through a fixed main sequence of slides and to answer correctly each question posed in the course of this sequence. He may avail himself of supplementary material for each question of the main sequence which he finds troublesome (help sequences). Further details of the teaching logic are illustrated in Fig. 3 and discussed in the following paragraphs.

Some slides of the main sequence contain only expository material ("text" slides). A text slide is shown in Fig. 4. When a student has finished reading a text slide, he pushes a button on his keyset labelled CONTINUE and the computer commands the slide selector to display the next slide of the sequence to this student. Just as the continue button enables the student to advance through the material, he can return to any previous slide by pushing the REVERSE key.

3-

EACH POSITIVE INTEGER IS REPRESENTED IN DECIMAL NOTATION BY COMBINING THE TEN DIGITS:

0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

THUS THE SYMBOL '3,549' IS INTERPRETED TO MEAN:

$3 \times 10^3 + 5 \times 10^2 + 4 \times 10 + 9$

i.e., $3 \times 1000 + 5 \times 100 + 4 \times 10 + 9$.

Fig. 4. Text slide

In addition to text slides, the main sequence will contain slides on which one or more questions are posed to the student. Spaces are provided on the slide for the student's answers (cf. Fig. 5). A student must answer each question correctly before he is permitted to continue to

QUESTION: GIVE THE POSITIVE, NON-TRIVIAL DIVISORS OF 51 IN INCREASING ORDER.

$d_1 =$ ____

$d_2 =$ ____

Fig. 5. Answer slide

the next slide. An attempt to bypass a slide with unanswered questions causes the computer to ring a bell indicating a fault. If, at some later time, the student should return to this slide (via REVERSE), his correct answers will again be displayed in their proper places.

The student types his answer to a question on the keyset. As he depresses each key, ILLIAC plots the corresponding character for display in the appropriate place on the television screen. Upon completing his answer, the student pushes the JUDGE button, and the computer writes either OK or NO next to his answer (cf. Fig. 6). Methods of judging answers are described below. If the answer is judged incorrect, the student may submit another answer to the question. To do this, he first erases his incorrect answer by depressing the ERASE key and then types his revised answer on the keyset. Upon request, just as before, the computer will judge the new answer.

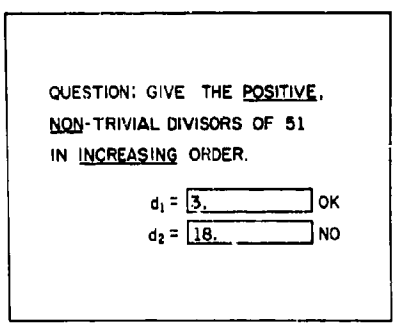

Fig. 6. Answer slide, filled-in and judged

A student is allowed as many tries as he likes in answering a question. In trying to answer a question a student is permitted to use the REVERSE button to review past material. If he still has difficulty answering a question, he may obtain supplementary material by depressing the HELP button. This action causes the computer to transfer from the main sequence of slides to the beginning of the appropriate help sequence. A help sequence, designed to lead the student to an understanding of the main-sequence problem, is provided for every question in the main sequence. The help sequence may contain a review and reformulation of previous materials pertinent to the question as well as suitable hints and suggestions. Often, a help sequence breaks the main-sequence problem down into a series of simpler problems, each of which the student presumably can work. The rules for proceeding along a help sequence are the same as those governing the main sequence; the student moves forward by use of the CONTINUE button, but must answer successfully each question posed in the sequence.

Memory limitations of ILLIAC preclude the use of secondary help sequences. Thus, if a student cannot submit a correct answer to a help-sequence problem and asks for help once more, the machine informs him that no additional help is available. He is given two alternatives: pushing REVERSE will return him to the problem for further consideration; pushing HELP (i.e., giving up) will cause the machine to provide him with the correct answer.

At the end of a help sequence, the CONTINUE button automatically returns the student to the main-sequence slide from which he came. It is expected that he can now answer the main-sequence problem and proceed. Otherwise, a renewed request for help will cause the machine to provide the student with the correct answer as described.

A student who has asked for help, may, as he proceeds through a help sequence, suddenly realize the answer to the main-sequence question. By pushing the AHA button he will be returned to the main-sequence problem and may try his new answer. If it is correct, he is permitted to proceed in the main sequence. Otherwise, a renewed request for help causes the machine to return him to the point in the help sequence at which he broke off. Thus, a student is not required to go through supplementary material which he does not feel he needs.

Answers may be judged in many ways. For questions having unique, well-defined answers, the computer compares the student's answer against the pre-stored correct answer. For numerical answers, tolerances may be specified. In more sophisticated judging routines, the computer itself determines the correctness of a student's answer by using it in suitable calculations. This approach is especially useful for questions permitting a variety of correct answers. Though not yet implemented, it appears desirable that the computer not merely judge an answer, but that it also examine each wrong answer for specific errors and route the student to special help sequences associated with each kind of error.

Finally, in addition to exercising the executive control associated with instruction, the program keeps accurate records of the moves made by each student and the time elapsed at each move. Thus, a wealth of precise and reliable data is available concerning each student's

progress through a lesson. At a later time, the computer can procers these data so as to reveal important information both about the students and lessons.

The Multiplexing Problem

The multiplexing of several students onto one computer is complicated by the problem of bookkeeping and time-sharing. The bookkeeping problem is easily solved. Most of the program is written to handle one student. All data for each student required by the program are kept together in a list. When the computer must turn its attention from one student to another, it saves the current information list and transfers the new information list from storage. This transfer of data lists is necessary because ILLIAC lacks index registers. ILLIAC's memory capacity, in addition, limits the current PLATO II to two students.

The problem of time-sharing is more difficult. Students tend to become confused if the computer does not respond immediately to their commands. For example, suppose a given student is typing his answer to a question and is unaware of the computer's availability to him. Then if other students have tied up the central computer, some of the characters in the answer will be lost. Care must be taken, therefore, to avoid situations where the computer is tied up except for brief periods.

The problem can be alleviated to some extent by the design of the equipment external to the computer. By providing a small amount of control circuitry at each student position, the system can perform some functions for the students in parallel. For example, the computer can tell the control circuit provided for a given student to erase his blackboard. The computer is then free to do operations for other students while the control circuit completes erasing. When the erase cycle is completed, the control circuit so informs the computer.

Further solution of the time-sharing problem must be obtained by the computer program itself. Clearly, the computer cannot be tied to a given student more than a certain maximum time. The reciprocal of this time limit defines a minimum rate at which the computer can accept information. Let us determine this rate. A student typing at a peak rate of 60 words per minute will generate one character per 200 milliseconds. The computer must accept information at this rate for n students, or at the rate of one character per 200/n milliseconds. This time is the upper limit that the program can operate without interrogating the keysets. In the computer program for PLATO II (where n = 2), the critical time limit is 100 milliseconds. For this program no input operations and only two output operations exceed the critical limit. One of these—erasing a given storage tube—has already been mentioned.

The other operation which exceeds the critical limit is that of plotting more than one character on a storage tube. For example, a student may return to a page of the lesson which he has already entered answers. His storage tube must first be erased, and the old answers must then be plotted on it. When this case arises, the program switches to a special mode of operation for the student in question called "unfinished business." In unfinished business, the computer is permitted to plot only one of the characters at a time before scanning all of the other keysets for possible inputs and performing any operations which these inputs may require. The student requiring unfinished business, then, is relegated to a position of lower priority, and the computer completes the student's unfinished business when it is receiving no inputs. The student's keyset is locked out during this time so that he cannot enter information inadvertently. In case of simultaneous unfinished business, students are disposed of one by one in the order in which unfinished business was required for each of them. It is thus possible for two students to share ILLIAC and, except when unfinished business is required, never experience delays due to equipment tieup.

Summary

The important feature of PLATO II are:

1. Each student may proceed through the material in a manner and at a speed of his own choosing, subject only to the boundary condition that he must solve successfully a prescribed sequence of problems. He may submit as many or as few answers to a question and seek as much or little supplementary material as he likes. It was felt that one cannot know a priori the particular needs of a student at any point in his progress through the material as well as the student himself. If the main sequence is written for the best students, the help sequences for the poorest ones, then each student may use the HELP and AHA keys to find for himself a suitable path in the spectrum between these two extremes.

2. The machine will accept and display constructed answers, as well as the more restrictive answers to multiple choice questions. The student is told as soon as he has submitted an answer, whether it is correct or incorrect. In the latter case, the machine can indicate NO

without revealing the correct solution. Also, since a student cannot proceed before answering a question correctly, the answer to any question may be used in the textual material of subsequent parts of the sequence. Finally, if the student reviews by means of the REVERSE key, his answers to questions on previous slides are again automatically displayed by the machine; the slide sequence now assumes the character of a filled-in work book.

3. The equipment, as well as the programmed logic, appear to be sufficiently versatile so that one can change from one subject matter to another by simply replacing slides in the slide selector and giving the computer a new set of parameters. Sequences of material involving subject matter that varies as widely as number theory and French grammar have been prepared for use with the same computer program.

For the purpose of providing an instrument for research in education, the following points seem to be particularly important:

1. The material is presented to every student in a standard, objective fashion.

2. At the end of any lesson, the experimenter has at his disposal a complete record of the student's progress through the material. It is hoped that such records, after suitable processing on the machine, will not only provide information about each student, but will be of use in revising the material taught.

Studies employing the PLATO II teaching logic indicate that the following additional feature would be an improvement: with the current logic, as soon as the student gets a problem right, no matter by what means, he is sent on to the next order of business. However, it now seems clear that in determining whether to proceed, the computer should take into account how the student came to the correct answer to a question. Three factors seem to be of importance:

1. How much time was required to solve the problem?

2. How many wrong answers were submitted?

3. Was help required?

On the basis of these three factors, the computer should decide whether to go on to the next point in the main sequence or continue to dwell on the current problem.